CLAIMS

1. An apparatus comprising:

a plurality of processors, each processor having the capability of executing a plurality of threads;

a memory coupled to the plurality of processors; and

a thread dispatch mechanism residing in the memory and executed by at least one of the plurality of processors, the thread dispatch mechanism determining which of the plurality of processors are idle, which of the plurality of processors can accept an additional thread, and which of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism dispatching a new thread to an idle processor, if one exists.

2. The apparatus of claim 1 wherein, if none of the plurality of processors is idle and if at least one of the plurality of processors can accept an additional thread, the thread dispatch mechanism dispatches the new thread to one of the plurality of processors that can accept an additional thread.

3. The apparatus of claim 1 wherein, if all of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism waits for one of the plurality of processors to complete processing a thread, thereby becoming a processor that can accept an additional thread, and then dispatches the thread to the processor that can accept an additional thread.

4. A method for dispatching threads in a computer system that includes a plurality of processors that can each execute a plurality of threads, the method comprising the steps of:

(1) determining the status of each of the plurality of processors, wherein a processor is idle if not executing any threads, wherein the processor can accept an additional thread if busy working on one or more threads but has the capacity to process the additional thread, and wherein the processor cannot accept an additional thread if busy working on a maximum number of threads the processor can execute; and

(2) dispatching a new thread to an idle processor, if one exists.

5. The method of claim 4 further comprising the step of:

if none of the plurality of processors is idle and if at least one of the plurality of processors can accept an additional thread, the thread dispatch mechanism dispatches the new thread to one of the plurality of processors that can accept an additional thread.

6. The method of claim 4 further comprising the steps of:

if all of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism waits for one of the plurality of processors to complete processing a thread, thereby becoming a processor that can accept an additional thread, and then dispatches the thread to the processor that can accept an additional thread.

7. A program product comprising:

(A) a thread dispatch mechanism that determines which of a plurality of processors in a multiprocessor computer system are idle, which of the plurality of processors can accept an additional thread, and which of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism dispatching a new thread to an idle processor, if one exists, wherein each processor can execute a plurality of threads; and

(B) computer-readable signal bearing media bearing the thread dispatch mechanism.

8. The program product of claim 7 wherein the computer-readable signal bearing media comprises recordable media.

9. The program product of claim 7 wherein the computer-readable signal bearing media comprises transmission media.

10. The program product of claim 7 wherein, if none of the plurality of processors is idle and if at least one of the plurality of processors can accept an additional thread, the thread dispatch mechanism dispatches the new thread to one of the plurality of processors that can accept an additional thread.

11. The program product of claim 7 wherein, if all of the plurality of processors cannot accept an additional thread, the thread dispatch mechanism waits for one of the plurality of processors to complete processing a thread, thereby becoming a processor that can accept an additional thread, and then dispatches the thread to the processor that can accept an additional thread.

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